IN THE CLAIMS:

The text of all pending claims (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please ADD new claims 11-26 in accordance with the following:

1 through 10 (CANCELLED)

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11. (NEW) A processor execution pipeline, comprising:

a first instruction decoding unit that decodes a first instruction into a first control signal, and decodes instructions with the exception of the first instruction into a second control signal;

a first processing unit that performs a first operation on a first data when receiving the first control signal, and passes the first data when receiving the second control signal;

a second instruction decoding unit that decodes a second instruction into a third control signal, and decodes instructions with the exception of the second instruction into a fourth control signal;

a second processing unit that performs a second operation on a second data when receiving the third control signal where the second data is an output of the first processing unit; and

a multiplexer that selects an output of the second processing unit or the second data.

12. (NEW) The processor execution pipeline according to claim 11, wherein

the multiplexer selects an output of the second processing unit when receiving the third control signal, and selects the second data when receiving the fourth control signal.

13. (NEW) The processor execution pipeline according to claim 11, further comprising:

a latching unit that holds the output of the first processing unit where the second data is data held by the latching unit.

14. (NEW) The processor execution pipeline according to claim 11, wherein the first processing unit receives multiple data as the first data.

15. (NEW) A processor execution pipeline, comprising:

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a first instruction decoding unit that decodes a first instruction into a first control signal, and decodes instructions with the exception of the first instruction into a second control signal;

a first processing unit that performs a first operation on a first data when receiving the first control signal;

a multiplexer that selects an output of the first processing unit or the first data;

a second instruction decoding unit that decodes a second instruction into a third control signal, and decodes instructions with the exception of the second instruction into a fourth control signal; and

a second processing unit that performs a second operation on a second data when receiving the third control signal, and passes the second data when receiving the fourth control signal, where the second data is an output of the multiplexer.

16. (NEW) The processor execution pipeline according to claim 15, wherein

the multiplexer selects an output of the first processing unit when receiving the first control signal, and selects the first data when receiving the second control signal.

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17. (NEW) The processor execution pipeline according to claim 18, further comprising:

a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit.

18. (NEW) The processor execution pipeline according to claim 15, wherein

the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data.

19. (NEW) A processor execution pipeline, comprising:

a first instruction decoding unit that decodes a first instruction into a first control signal, and decodes instructions with the exception of the first instruction into a second control signal;

a first processing unit that performs a first operation on a first data when receiving the first control signal, and passes the first data when receiving the second control signal;

a second instruction decoding unit that decodes the first instruction into a third control signal, decodes a second instruction into a fourth control signal, and decodes instructions with

the exception of the first and second instructions into a fifth control signal;

A16 a second processing unit that performs a second operation on a second data when receiving the third control signal, and performs a third operation on the second data when receiving the fourth control signal, where the second data is an output of the first processing unit; and

a multiplexer that selects an output of the second processing unit or the second date.

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20. (NEW) The processor execution pipeline according to claim ~~18~~, wherein

the multiplexer selects an output of the second processing unit when receiving either one of the third or the fourth control signals, and selects the second data when receiving the fifth control signal.

21. (NEW) The processor execution pipeline according to claim 19, further comprising:

a latching unit that holds the output of the first processing unit, where the second data is data held by the latching unit.

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22. (NEW) The processor execution pipeline according to claim ~~18~~, wherein the first processing unit receives multiple data as the first data.

23. (NEW) A processor execution pipeline, comprising:

a first instruction decoding unit that decodes a first instruction into a first control signal, decodes a second instruction into a second control signal, and decodes instructions with the exception of the first and second instructions into a third control signal;

a first processing unit that performs a first operation on a first data when receiving the first control signal, and performs a second operation on the first data when receiving the second control signal;

a multiplexer that selects an output of the first processing unit or the first data;

a second instruction decoding unit that decodes the first instruction into a fourth control signal, and decodes instructions with the exception of the first instruction into a fifth control signal; and

a second processing unit that performs a third operation on a second data when receiving the fourth control signal, and passes the second data when receiving the fifth control signal, where the second data is an output of the multiplexer.

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24. (NEW) The processor execution pipeline according to claim 23, wherein

the multiplexer selects an output of the first processing unit when receiving either one of the first or the second control signals, and selects the first data when receiving the third control signal.

25. (NEW) The processor execution pipeline according to claim 23, further comprising:

a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit.

26. (NEW) The processor execution pipeline according to claim 23, wherein

the first processing unit receives multiple data as the first data, and

the multiplexer receives the output of the first operating unit and one of the multiple data.